

ATSAME70Q21B-ANT

Data Sheet

RFO

MCU 32-bit ARM Cortex M7 RISC 2MB Flash 1.8V/2.5V/3.3V 144-Pin LQFP T/R

Manufacturers	Microchip Technology, Inc	Contraction of the second s
Package/Case	LQFP-144	annuman
Product Type	Embedded Processors & Controllers	And the second s
RoHS		
Lifecycle		Images are for reference only

Please submit RFQ for ATSAME70Q21B-ANT or Email to us: sales@ovaga.com We will contact you in 12 hours.

General Description

The MicrochipSAME70Q21 devices are members of a flash microcontrollers family based on the high-performance 32-bit ARM Cortex-M7 processor with Floating Point Unit (FPU). These devices operate at up to 300MHz and feature up to 2048 Kbytes of Flash, up to 384 Kbytes of multi-port SRAM and configurable Instruction and Data Tightly Couple Memories to leverage the advanced DSP capabilities of the core. SAME70Q21 features multiple networking/connectivity peripherals, including CAN-FD interface and one 10/100Mbps Ethernet MAC with specific hardware support for Audio Video Bridging (AVB). Additional communication interfaces include a HS USB Host and Device, a HS SDCard/SDIO/MMC interface, USARTs, SPIs and multiple TWIs.Analog features include dual 2Msps 12-bit ADCs with analog front end offering offset and gain error correction, and 2Msps 12-bit DAC.

The SAME70Q21 is available in 144-pin QFP and BGA package options.

Note: While there are no plans to change the availabilitystatus of Revision A for this device, new designs should use Revision B for prototypes and production. Supported by MPLAB X IDE and MPLAB Harmony.

Features

Core

ARM® Cortex®-M7 running up to 300MHz

16 Kbytes of ICache and 16 Kbytes of DCache with Error Code Correction (ECC)

Single- and double-precision HW Floating Point Unit (FPU)

Memory Protection Unit (MPU) with 16 zones

DSP Instructions, Thumb®-2 Instruction Set

Embedded Trace Module (ETM) with instruction trace stream, including Trace Port Interface Unit (TPIU)

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Memories

2048 Kbytes embedded Flash with unique identifier and user signature for user-defined data

384 Kbytes embedded Multi-port SRAM

Tightly Coupled Memory (TCM) interface with four configurations (disabled, 2 x 32 Kbytes, 2 x 64 Kbytes, 2 x 128 Kbytes)

16 Kbytes ROM with embedded Bootloader routines (UARTO, USB) and IAP routines

16-bit Static Memory Controller (SMC) with support for SRAM, PSRAM, LCD module, NOR and NAND Flash with on-the-fly scrambling

16-bit SDRAM Controller (SDRAMC) interfacing up to 256 MB and with on-the-fly scrambling

System

Embedded voltage regulator for single-supply operation

Power-on-Reset (POR), Brown-out Detector (BOD) and Dual Watchdog for safe operation

Quartz or ceramic resonator oscillators: 3 to 20 MHz main oscillator with failure detection, 12 MHz or 16 MHz needed for USB operations. Optional low-power 32.768 kHz for RTC or device clock

RTC with Gregorian calendar mode, waveform generation in low-power modes

RTC counter calibration circuitry compensates for 32.768 kHz crystal frequency variations

32-bit low-power Real-time Timer (RTT)

High-precision Main RC oscillator with 12 MHz default frequency for device startup. In-application trimming access for frequency adjustment. 8/12 MHz are factory-trimmed.

32.768 kHz crystal oscillator or Slow RC oscillator as source of low-power mode device clock (SLCK)

One 500 MHz PLL for system clock, one 480 MHz PLL for USB high-speed operations

Temperature Sensor

One dual-port 24-channel central DMA Controller (XDMAC)

Low-Power Features

Low-power Sleep, Wait and Backup modes, with typical power consumption down to 1.1 µA in Backup mode with RTC, RTT and wakeup logic enabled

Ultra-low-power RTC and RTT

1 Kbyte of backup RAM (BRAM) with dedicated regulator

Peripherals

One Ethernet MAC (GMAC) 10/100 Mbps in MII mode and RMII with dedicated DMA. IEEE1588 PTP frames and 802.3az Energyefficiency support. Ethernet AVB support with IEEE802.1AS Timestamping and IEEE802.1Qav credit-based traffic-shaping hardware support

USR 2.0 Device/Mini Host Hioh-speed (USRHS) at 480 Mbns. 4-K hvte FIFO_un to 10 bidirectional endpoints. dedicated DMA

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12-bit ITU-R BT. 601/656 Image Sensor Interface (ISI)

Two master Controller Area Networks (MCAN) with Flexible Data Rate (CAN-FD) with SRAM-based mailboxes, time- and event-triggered transmission

ISO CAN FD; ISO 1189801:2015 (Revision B only)

Three USARTs. USART0/1/2 support LIN mode, ISO7816, IrDA®, RS-485, SPI, Manchester and Modern modes; USART1 supports LON mode.

Five 2-wire UARTs with SleepWalking[™] support

Three Two-Wire Interfaces (TWIHS) (I2C-compatible) with SleepWalking™ support

Quad I/O Serial Peripheral Interface (QSPI) interfacing up to 256 MB Flash and with eXecute-In-Place and on-the-fly scrambling

Two Serial Peripheral Interfaces (SPI)

One Serial Synchronous Controller (SSC) with I2S and TDM support

Two Inter-IC Sound Controllers (I2SC)

One High-speed Multimedia Card Interface (HSMCI) (SDIO/SD Card/e.MMC)

Four Three-Channel 16-bit Timer/Counters (TC) with Capture, Waveform, Compare and PWM modes, constant on time. Quadrature decoder logic and 2-bit Gray Up/Down Counter for stepper motor

Two 4-channel 16-bit PWMs with complementary outputs, Dead Time Generator and eight fault inputs per PWM for motor control, two external triggers to manage power factor correction (PFC), DC-DC and lighting control.

Two Analog Front-End Controllers (AFEC), each supporting up to 12 channels with differential input mode and programmable gain stage, allowing dual sample-and-hold at up to 1.7 Msps. Offset and gain error correction feature.

One 2-channel 12-bit 1 Msps-per-channel Digital-to-Analog Controller (DAC) with Differential and Over Sampling modes

One Analog Comparator Controller (ACC) with flexible input selection, selectable input hysteresis

Cryptography

True Random Number Generator (TRNG)

AES: 256-, 192-, 128-bit Key Algorithm, Compliant with FIPS PUB-197 Specifications

Integrity Check Monitor (ICM). Supports Secure Hash Algorithm SHA1, SHA224 and SHA256.

I/O

Up to 114 I/O lines with external interrupt capability (edge- or level-sensitivity), debouncing, glitch filtering and On-die Series Resistor Termination

Five Parallel Input/output Controllers (PIO)

Voltage

Single Cumuker waltage from 1 71/ to 2 61/ for Industrial Tomas water Darris

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Packages

LQFP144, 144-lead LQFP, 20 x 20 mm, pitch 0.5 mm LFBGA144, 144-ball TFBGA, 10 x 10 mm, pitch 0.8 mm UFBGA144, 144-ball UFBGA, 6 x 6 mm, pitch 0.4 mm

Related Products



ATSAMA5D36A-CU Microchip Technology, Inc LFBGA-324



ATXMEGA128D3-AU Microchip Technology, Inc TQFP-64



ATMEGA64M1-15AZ Microchip Technology, Inc TQFP-32



ATTINY48-MU Microchip Technology, Inc VQFN-32









SOIC-20 ATMEGA16L-8PU

ATTINY2313V-10SU

Microchip Technology, Inc

ATMEGA32M1-AU

TQFP-32

Microchip Technology, Inc

Microchip Technology, Inc PDIP-40

ATTINY4-TSHR

Microchip Technology, Inc SOT-23-6

