

2-Channel Dual ADC Pipelined 250MSPs 14-bit Serial 48-Pin LFCSP EP Tray

Manufacturers	<u>Analog Devices, Inc</u>
Package/Case	LFCSP-48
Product Type	Data Conversion ICs
RoHS	Rohs
Lifecycle	



Images are for reference only

Please submit RFQ for AD9250BCPZ-250 or [Email to us: sales@ovaga.com](mailto:sales@ovaga.com) We will contact you in 12 hours.

[RFQ](#)

General Description

The AD9250 is a dual, 14-bit ADC with sampling speeds of up to 250 MSPS. The AD9250 is designed to support communications applications where low cost, small size, wide bandwidth, and versatility are desired.

The ADC cores feature a multistage, differential pipelined architecture with integrated output error correction logic. The ADC cores feature wide bandwidth inputs supporting a variety of user-selectable input ranges. An integrated voltage reference eases design considerations. A duty cycle stabilizer is provided to compensate for variations in the ADC clock duty cycle, allowing the converters to maintain excellent performance. The JESD204B high speed serial interface reduces board routing requirements and lowers pin count requirements for the receiving device.

By default, the ADC output data is routed directly to the two JESD204B serial output lanes. These outputs are at CML voltage levels. Four modes support any combination of = 1 or 2 (one or two lanes). For dual ADC mode, data can be sent through two lanes at the maximum sampling rate of 250 MSPS. However, if data is sent through one lane, a sampling rate of up to 125 MSPS is supported. Synchronization inputs (SYNCIN± and SYSREF±) are provided.

Flexible power-down options allow significant power savings, when desired. Programmable overrange level detection is supported for each channel via the dedicated fast detect pins.

Programming for setup and control are accomplished using a 3-wire SPI-compatible serial interface.

The AD9250 is available in a 48-lead LFCSP and is specified over the industrial temperature range of -40°C to +85°C.

Product Highlights

Applications

Integrated dual, 14-bit, 170 MSPS/250 MSPS ADC.

The configurable JESD204B output block supports up to 5 Gbps per lane.

An on-chip, phase-locked loop (PLL) allows users to provide a single ADC sampling clock; the PLL multiplies the ADC sampling clock to produce the corresponding JESD204B data rate clock.

Support for an optional RF clock input to ease system board design.

Proprietary differential input maintains excellent SNR performance for input frequencies of up to 400 MHz.

Operation from a single 1.8 V power supply.

Standard serial port interface (SPI) that supports various product features and functions such as controlling the clock DCS, power-down, test modes, voltage reference mode, over range fast detection, and serial output configuration.

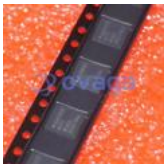
Features

Application

JESD204B Subclass 0 or Subclass 1 coded serial digital outputs	Diversity radio systems
Signal-to-noise ratio>	Multimode digital receivers (3G)
Spurious-free dynamic range>	TD-SCDMA, WiMAX, W-CDMA, CDMA2000, GSM, EDGE, LTE
Total power consumption: 711 mW at 250 MSPS	DOCSIS 3.0 CMTS upstream receive paths
1.8 V supply voltages	HFC digital reverse path receivers
Integer 1-to-8 input clock divider	I/Q demodulation systems
Sample rates of up to 250 MSPS	Smart antenna systems
IF sampling frequencies of up to 400 MHz	Electronic test and measurement equipment
Internal analog-to-digital converter (ADC) voltage reference	Radar receivers
Flexible analog input range	COMSEC radio architectures
1.4 V p-p to 2.0 V p-p (1.75 V p-p nominal)	IED detection/jamming systems
ADC clock duty cycle stabilizer (DCS)	General-purpose software radios
95 dB channel isolation/crosstalk	Broadband data applications
Serial port control	TD-SCDMA, WiMAX, W-CDMA, CDMA2000, GSM, EDGE, LTE
Energy saving power-down modes	
1.4 V p-p to 2.0 V p-p (1.75 V p-p nominal)	

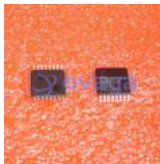


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LFCSP-40



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TQPF-32



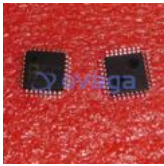
[AD574AJNZ](#)

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