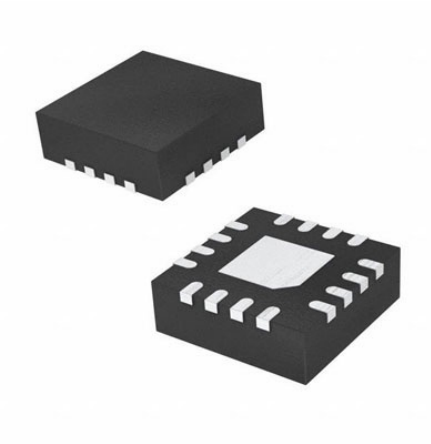
1894K-32LFT

Data Sheet

PHYCEIVER LOW PWR 3.3V 32QFN; HT SUSA CODE:8542390000

Manufacturers	Renesas Technology Corp
Package/Case	32-VFQFN
Product Type	Interface ICs
RoHS	Rohs
Lifecycle	



Images are for reference only

Please submit RFQ for 1894K-32LFT or Email to us: sales@ovaga.com We will contact you in 12 hours.

RFQ

General Description

The IDT1894-32 is a low-power, physical-layer device (PHY) that supports the ISO/IEC 10Base-T and 100Base-TX Carrier-Sense Multiple Access/Collision Detection (CSMA/CD) Ethernet standards, ISO/IEC 8802-3.The IDT1894-32 is intended for MII, Node applications that require the Auto-MDIX feature that automatically corrects crossover errors in plant wiring.The IDT1894-32 incorporates Digital-Signal Processing (DSP) control in its Physical-Medium Dependent (PMD) sub layer. As a result, it can transmit and receive data on unshielded twisted-pair (UTP) category 5 cables with attenuation in excess of 24 dB at 100MHz. With this IDT-patented technology, the IDT1894-32 can virtually eliminate errors from killer packets.The IDT1894-32 provides a Serial-Management Interface for exchanging command and status information with a Station-Management (STA) entity. The IDT1894-32 Media-Dependent Interface (MDI) can be configured to provide either half- or full duplex operation at data rates of 10 Mb/s or 100Mb/s.In addition, the IDT1894-32 includes a programmable interupt output function. This function consists of a digital output pin, an interrupt control register, a set of interrupt status register bits and a corresponding set of interrupt enable bits, and a pre-defined set of events which can be assigned as one of the interrupt sources. The purpose of this function is to notify the host of this PHY device when certain event happens via interrupt (the logic level on interrupt output pin going low or going high) instead of polling by the host. The events that could be used to generate interrupts are: receiver error, Jabber, page received, parallel detect fault, link partner acknowledge, link status change, auto-negotiation complete, remote fault, collision, etc.**Applications**: NIC cards, PC motherboards, switches, routers, DSL and cable modems, game machines, printers, network connected appliances, and industrial equipment.

Features

Supports category 5 cables with attenuation in excess of 24dB at 100 MHz.

Single-chip, fully integrated PHY provides PCS, PMA, PMD, and AUTONEG sub layers functions of IEEE standard.

10Base-T and 100Base-TX IEEE 8802.3 compliant

MIIM (MDC/MDIO) management bus for PHY register configuration

RMII interface support with external 50 MHz system clock

Single 3.3V power supply

Highly configurable

Media Independent Interface (MII)

Auto-Negotiation with Parallel detection

Node applications, managed or unmanaged

10M or 100M full and half-duplex modes

Loopback mode for Diagnostic FunctionsAuto-MDI/MDIX crossover correction

Low-power CMOS (typically 300 mW)

Power-Down mode typically 21mW

Clock and crystal supported

Interrupt pin option

Fully integrated, DSP-based PMDAdaptive equalization and baseline-wander correction

Transmit wave shaping and stream cipher scrambler

MLT-3 encoder and NRZ/NRZI encoder

Single power supply (3.3 V)

Built-in 1.8 V regulator for core

Available in 32-pin (5mm x 5mm) QFN package, Pb-free

Available in Industrial Temp and Lead Free

Related Products

[HS1-3182-8]

Renesas Technology Corp

DIP16

[1893CFLFT]

Renesas Technology Corp

SSOP48

[HA12187]

Renesas Technology Corp

SOP8

[HA12187FP]

Renesas Technology Corp

SOP8

[ISL3180EIBZ]

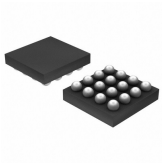
Renesas Technology Corp

SOIC-14

[HS1-3182-9+]

Renesas Technology Corp

16-CDIP (0.300, 7.62mm)



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Renesas Technology Corp

34-UFBGA, WLCSP

[1893BFLF]

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SSOP-48