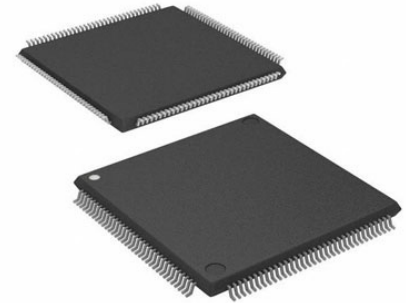


ARM MCU, SAM4E Series, SAM32 Family SAM 4E Series Microcontrollers, ARM Cortex-M4, 32bit, 120 MHz

Manufacturers	Microchip Technology, Inc
Package/Case	LQFP-144
Product Type	Embedded Processors & Controllers
RoHS	Green
Lifecycle	



Images are for reference only

Please submit RFQ for ATSAM4E16EA-AU or [Email to us: sales@ovaga.com](mailto:sales@ovaga.com) We will contact you in 12 hours.

[RFQ](#)

General Description

For New Designs, we highly recommend to consider Revision B for Prototypes and Production.

ARM® Cortex®-M4 processor-based microcontroller (MCU), the SAM4E16E features a floating point unit and a high data bandwidth architecture and is targeted at industrial automation and building control applications.

The device embeds 1MB Flash and features multiple networking/connectivity peripherals, including two 2.0A/B compatible CAN interfaces and an IEEE Std 1588-compatible 10/100Mbps Ethernet MAC. Additional communication interfaces include a FS USB device, a HS SDCard/SDIO/MMC interface, USARTs, SPIs and multiple TWIs.

Analog features include dual 1Msps, 16-bit ADCs of up to 24 channels with analog front end offering offset and gain error correction, and a 2-channel, 1Msps, 12-bit DAC.

The SAM4E16E is available in 144-pin BGA and QFP package options.

Features

Microcontroller Features

Core

ARM Cortex-M4 with 2 Kbytes Cache running at up to 120 MHz

Memory Protection Unit (MPU)

DSP Instructions, Floating Point Unit (FPU), Thumb®-2 instruction set

Memories

1024 Kbytes Embedded Flash

128 Kbytes Embedded SRAM

16 Kbytes ROM with Embedded Boot Loader Routines (UART) and IAP Routines

Static Memory Controller (SMC): SRAM, NOR, NAND Support

NAND Flash Controller

System

Embedded voltage regulator for single-supply operation

Power-on-Reset (POR), Brown-out Detector (BOD) and Dual Watchdog for Safe Operation

Quartz or ceramic resonator oscillators: 3 to 20 MHz with clock failure detection and 32.768 kHz for RTT or system clock

RTC with Gregorian and Persian Calendar Mode, Waveform Generation in Backup mode

RTC counter calibration circuitry compensates for 32.768 kHz crystal frequency inaccuracy

High-precision 8/16/24 MHz factory-trimmed internal RC oscillator. In-application trimming access for frequency adjustment

Slow clock internal RC oscillator as permanent low-power mode device clock

One PLL up to 240 MHz for Device Clock and for USB

Temperature Sensor

Low-power tamper detection on two inputs, anti-tampering by immediate clear of general-purpose backup registers (GPBR)

Up to 2 Peripheral DMA Controllers (PDC) with up to 33 Channels

One 4-channel DMA Controller

Low Power modes

Sleep, Wait and Backup modes, down to 0.9 μ A in Backup mode with RTC, RTT, and GPBR

Package

144-ball LFBGA, 10x10 mm, pitch 0.8 mm

144-lead LQFP, 20x20 mm, pitch 0.5 mm

Temperature operating range

Revision A - Industrial (-40° C to +85° C), Revision B -(-40° C to +105° C)

Peripheral Features

Two USARTs with USART1 (ISO7816, IrDA®, RS-485, SPI, Manchester and Modem Modes)

USB 2.0 Device: Full Speed (12 Mb/s), 2668 byte FIFO, up to 8 Endpoints. On-chip Transceiver

Two 2-wire UARTs

Two 2-wire Interfaces (TWI)

High-speed Multimedia Card Interface (SDIO/SD Card/MMC)

One Master/Slave Serial Peripheral Interface (SPI) with Chip Select Signals

Three 3-channel 32-bit Timer/Counter blocks with Capture, Waveform, Compare and PWM Mode. Quadrature Decoder Logic and 2-bit Gray Up/Down Counter for Stepper Motor.

32-bit low-power Real-time Timer (RTT) and low-power Real-time Clock (RTC) with calendar and alarm features

256-bit General Purpose Backup Registers (GPBR)

One Ethernet MAC (GMAC) 10/100 Mbps in MII mode only with dedicated DMA and Support for IEEE1588, Wake-on-LAN

Two CAN Controllers with eight Mailboxes

4-channel 16-bit PWM with Complementary Output, Fault Input, 12-bit Dead Time Generator Counter for Motor Control.

Real-time Event Management

I/O

Up to 117 I/O Lines with External Interrupt Capability (Edge or Level Sensitivity), Debouncing, Glitch Filtering

Bidirectional Pad, Analog I/O, Programmable Pull-up/Pull-down

Five 32-bit Parallel Input/Output Controllers, Peripheral DMA Assisted Parallel Capture Mode

Cryptography

AES 256-bit Key Algorithm compliant with FIPS Publication 197

Analog Features

AFE (Analog Front End): 2x16-bit ADC, up to 24-channels, Differential Input Mode, Programmable Gain Stage, Auto Calibration and Automatic Offset Correction

One 2-channel 12-bit 1 Msps DAC

One Analog Comparator with Flexible Input Selection, Selectable Input Hysteresis

Debugger Development Support

Serial Wire/JTAG Debug Port(SWJ-DP)

Debug access to all memories and registers in the system, including Cortex-M4 register bank when the core is running, halted, or held in reset.

Serial Wire Debug Port (SW-DP) and Serial Wire JTAG Debug Port (SWJ-DP) debug access.

Flash Patch and Breakpoint (FPB) unit for implementing breakpoints and code patches.

Data Watchpoint and Trace (DWT) unit for implementing watchpoints, data tracing, and system profiling.

Instrumentation Trace Macrocell (ITM) for support of printf style debugging

IEEE1149.1 JTAG Boundary-scan on all digital pins.

Integrated Software Libraries and Tools

ASF-Atmel software Framework – SAM software development framework

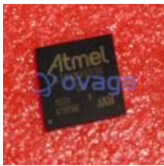
Integrated in the Atmel Studio IDE with a graphical user interface or available as standalone for GCC, IAR compilers.

DMA support, Interrupt handlers Driver support

USB, TCP/IP, Wi-Fi and Bluetooth, Numerous USB classes, DHCP and Wi-Fi encryption Stacks

RTOS integration, FreeRTOS is a core component

Related Products



[ATSAM5D36A-CU](#)

Microchip Technology, Inc
LFBGA-324



[ATMEGA32M1-AU](#)

Microchip Technology, Inc
TQFP-32



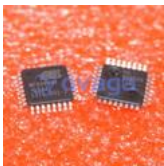
[ATXMEGA128D3-AU](#)

Microchip Technology, Inc
TQFP-64



[ATTINY2313V-10SU](#)

Microchip Technology, Inc
SOIC-20



[ATMEGA64M1-15AZ](#)

Microchip Technology, Inc
TQFP-32



[ATMEGA16L-8PU](#)

Microchip Technology, Inc
PDIP-40



[ATTINY48-MU](#)

Microchip Technology, Inc
VQFN-32



[ATTINY4-TSHR](#)

Microchip Technology, Inc
SOT-23-6