AD9162BBCAZ

Data Sheet

DAC 1-CH Quad-Switch 16-bit 169-Pin CSP-BGA Tray

Manufacturers	Analog Devices, Inc
Package/Case	169-VFBGA, CSPBGA
Product Type	Data Conversion ICs
RoHS	Pb-free Halide free
Lifecycle	

Images are for reference only

Please submit RFQ for AD9162BBCAZ or Email to us: sales@ovaga.com We will contact you in 12 hours. RFQ

General Description

The AD9162 is a high performance, 16-bit digital-to-analog converter (DAC) that supports data rates to 6 GSPS. The DAC core is based on a quad-switch architecture coupled with a 2× interpolator filter that enables an effective DAC update rate of up to 12 GSPS in some modes. The high dynamic range and bandwidth makes these DACs ideally suited for the most demanding high speed radio frequency (RF) DAC applications.

In baseband mode, wide bandwidth capability combines with high dynamic range to support DOCSIS 3.1 cable infrastructure compliance from the minimum of two carriers to full maximum spectrum of 1.794 GHz. A 2× interpolator filter (FIR85) enables the AD9161/AD9162 to be configured for lower data rates and converter clocking to reduce the overall system power and ease the filtering requirements. In Mix-Mode™ operation, the AD9161/AD9162 can reconstruct RF carriers in the second and third Nyquist zones up to 7.5 GHz while still maintaining exceptional dynamic range. The output current can be programmed from 8 mA to 38.76 mA. The AD9161/AD9162 data interface consists of up to eight JESD204B serializer/deserializer (SERDES) lanes that are programmable in terms of lane speed and number of lanes to enable application flexibility.

A serial peripheral interface (SPI) can configure the AD9161/AD9162 and monitor the status of all registers. The AD9161/AD9162 are offered in an 165-ball, 8.0 mm × 8.0 mm, 0.5 mm pitch, CSP_BGA package and in an 169-ball, 11 mm × 11 mm, 0.8 mm pitch, CSP_BGA package, including a leaded ball option for the AD9162.

Product Highlights

High dynamic range and signal reconstruction bandwidth supports RF signal synthesis of up to 7.5 GHz.

Up to eight lanes JESD204B SERDES interface flexible in terms of number of lanes and lane speed.

Bandwidth and dynamic range to meet DOCSIS 3.1 compliance with margin.

Features

DAC update rate up to 12 GSPS (minimum)

Direct RF synthesis at 6 GSPS (minimum)

DC to 2.5 GHz in baseband 1× bypass mode

DC to 6 GHz in 2× nonreturn-to-zero (NRZ) mode

1.5 GHz to 7.5 GHz in Mix-Mode

Bypassable interpolation (1× or bypass mode)

2×, 3×, 4×, 6×, 8×, 12×, 16×, 24×

Excellent dynamic performance

Application

Broadband communications systems

DOCSIS 3.1 cable modem termination system (CMTS)/video on demand (VOD)/edge quadrature amplitude modulation (EQAM)

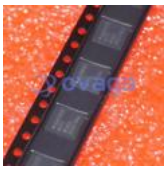
Wireless communications infrastructure

W-CDMA, LTE, LTE-A, point to point

Instrumentation, automatic test equipment (ATE)

Radars and jammers

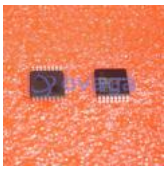
Related Products



ADAS3022BCPZ

Analog Devices, Inc

LFCSP-40



AD7266BSUZ

Analog Devices, Inc

TQPF-32

AD574AJNZ

Analog Devices, Inc

PDIP-28

AD7401YRWZ

Analog Devices, Inc

SOIC-16

AD7938BSUZ

Analog Devices, Inc

TQFP-32

AD7192BRUZ-REEL

Analog Devices, Inc

TSSOP-24

AD7124-8BCPZ-RL7

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LFCSP-32

AD9680BCPZ-500

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LFCSP-64